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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,674	03/30/2001	Hong Wang	42390.P10811	6127

7590

10/06/2004

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EXAMINER

BULLOCK JR, LEWIS ALEXANDER

ART UNIT

PAPER NUMBER

2127

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/823,674	<b>Applicant(s)</b> WANG ET AL.	
	<b>Examiner</b> Lewis A. Bullock, Jr.	<b>Art Unit</b> 2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 and 19-29 is/are rejected.
- 7) ☒ Claim(s) 17, 18, 30 and 31 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 13 is objected to because of the following informalities: the claim does not end in a period. Appropriate correction is required.
2. Claim 17 is objected to because of the following informalities: the claim seems to be missing some propositions, i.e. "and to decrement en the main thread", and details the word "en" on line 4. See indication of allowable subject matter for suggested corrections. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

3. Claim 10 recites the limitation "the speculative thread" in line 2. There is insufficient antecedent basis for this limitation in the claim. There exist a plurality of speculative threads. Therefore, it cannot be ascertained as to which thread Applicant refers to. If Applicant means that both threads are considered then the term "thread" should be "threads".

### ***Allowable Subject Matter***

4. Claims 17, 18, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
5. The following is a statement of reasons for the indication of allowable subject matter: The cited claims detail the limitations of using a outstanding pre-computation

Art Unit: 2126

slice counter to track for a set of loads of interest the number of speculative threads that have been spawned relative to the number of instances of any load of interest that have not yet been retired by the main thread and to decrement the counter if the main thread retires the corresponding load of interest. The prior art of record does not adequately teach this limitation. Prior art reference, TORII at best teaches spawning a speculative thread from a main thread and spawning another speculative thread from the speculative thread. Prior art references, "Speculative Data-Driven Multithreading" by ROTH and "Threaded Multiple Path Execution" by Wallace, at best teaches a main thread spawning multiple speculative threads to handling loads of interest and maintaining a counter of the loads of interest. However, the cited references teaches against performing this technique wherein a speculative thread spawns another speculative thread as is disclosed in the cited claims. Therefore, the stated claim language is allowable over the cited prior art of record both independent and in combination.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-5, 8-13, 15, 16, 19-23 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by TORII (U.S. Patent 6,389,446).

As to claim 1, TORII teaches a method comprising: dynamically invoking a speculative thread (thread 1 / child thread) from a main thread (thread 0 / parent thread) in a processor (via thread generation instruction) and executing instructions comprising the speculative thread (col. 13, lines 4-17).

As to claim 9, TORII teaches a method in a processor, comprising: dynamically invoking from a first speculative thread (thread 1 / child thread) a second speculative thread (thread 2 / subsequent child thread), wherein the first speculative thread is dynamically invoked from a main thread (thread 0 / parent thread); and executing instructions comprising the first and second speculative threads (col. 13, lines 4-17).

As to claim 13, TORII teaches a processor, comprising: a first hardware (processor) to store a main software thread (thread 0 / parent thread); a second hardware (processor) to store a speculative software thread (thread 1 / child thread) (col. 13, lines 4-17); logic (intra-thread processors communication bus) coupled between the first and second hardware (processors) (col. 10, lines 49-51) and a machine-readable medium having machine-readable instructions stored thereon to instruct a processor to bind the speculative software thread (child thread) to the second hardware (processor) (via the thread manager determining a free processor and

sending the thread start address to the available processor) (col. 5, lines 1-12; col. 6, lines 32 – col. 7, line 13) and to transfer live-in values (dependency data / start thread information) from main software thread to the speculative software thread (col. 9, lines 35-55). It would be inherent to the teachings of TORII that since the hardware has a hardware context, since the threads execute to completion on the hardware.

As to claim 15, TORII teaches a processor, comprising: a first hardware (processor) to store a main thread (thread 0 / parent thread); a second hardware (processor) and a third hardware (processor) to bind to a first speculative thread (thread 1/ child thread) and a second speculative thread (thread 2 / subsequent child thread), respectively, the main thread to dynamically invoke the first speculative thread and the first speculative thread to dynamically invoke the second speculative thread (col. 13, lines 4-17); and logic (intra-thread processors communication bus) coupled between the first, second, and third hardware (processors) (col. 10, lines 49-51), and a processor-readable medium having processor-readable instructions stored thereon to instruct the processor, to bind the first and second speculative threads to the second and third hardware (via the thread manager determining a free processor and sending the thread start address to the available processor) (col. 6, lines 32 – col. 7, line 13), respectively and to transfer live-in values (dependency data / start thread information) from main thread to the first speculative thread and from the first speculative thread to the second speculative thread (col. 9, lines 35-55), wherein the processor-readable medium includes at least one instruction to instruct the processor to trigger the invocation of the

Art Unit: 2126

first and second speculative threads (via the thread generation instructions) (col. 13, lines 4-17). It would be inherent to the teachings of TORII that since the hardware has a hardware context, since the threads execute to completion on the hardware.

As to claim 19, reference is made to a machine-readable medium that corresponds to the method of claim 1 and is therefore met by the rejection of claim 1 above.

As to claim 26, reference is made to a machine-readable medium that corresponds to the method of claim 9 and is therefore met by the rejection of claim 1 above.

As to claim 2, TORII teaches attempting to bind a hardware (processor) for the speculative thread (via the thread manager determining a free processor and sending the thread start address to the available processor) (col. 6, lines 32 – col. 7, line 13). It would be inherent to the teachings of TORII that since the hardware has a hardware context, since the threads execute to completion on the hardware.

As to claims 3-5, TORII teaches determining whether the attempt to bind the hardware (processor) for the speculative thread was a success or failure and reporting according (col. 9, lines 35-55).



Art Unit: 2126

As to claim 8, TORII teaches starting each speculative thread (thread start instruction) and executing the threads independently from the parent thread wherein if a processor is not available, allocating an entry in a queue (buffer) for a copy of at least one instruction (thread start instruction) until hardware becomes available. It would be inherent to the teachings of TORII that each thread has a pre-computation slice of instructions since the threads speculatively execute in parallel with one another. It is also inherent within the teachings of TORII that the pre-computed slice of instructions is identified from the start information.

As to claim 10, refer to claim 2 for rejection.

As to claim 11, TORII teaches detecting a trigger to invoke the second speculative thread (via thread start instruction), storing second speculative thread live-in values (data / thread start instruction) to a buffer (information buffer), and executing instructions in the second speculative thread (execute thread when assigned to a processor) (col. 10, lines 49 – col. 11, line 35).

As to claim 12, TORII teaches starting each speculative thread (thread start instruction) and executing the threads independently from the parent thread wherein if a processor is not available, allocating an entry in a queue (buffer) for a copy of at least one instruction (thread start instruction) until hardware becomes available. It would be

Art Unit: 2126

inherent to the teachings of TORII that each thread has a pre-computation slice of instructions.

As to claim 16, refer to claim 12 for rejection.

As to claim 20 and 23, refer to claim 12 for rejection.

As to claim 21, TORII teaches bind a hardware (processor) for the speculative thread (via the thread manager determining a free processor and sending the thread start address to the available processor) (col. 6, lines 32 – col. 7, line 13); transfer live-in values (thread start instruction / data) from the main thread to the speculative thread (col. 9, lines 35-55); and load live-in values in the hardware for the speculative thread (via executing the thread generating instruction on the processor) (col. 6, lines 32 – col. 7, line 13).

As to claim 22, refer to claim 8 for rejection.

As to claim 27, TORII teaches bind a hardware (processor) for the speculative threads (via the thread manager determining a free processor and sending the thread start address to the available processor) (col. 6, lines 32 – col. 7, line 13); transfer live-in values (thread start instruction / data) from the main thread to the speculative threads (col. 9, lines 35-55).

As to claim 28, refer to claim 8 for rejection.

As to claim 29, refer to claim 12 for rejection.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-6, 13, 14 and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Speculative Data-Driven Multithreading" by ROTH in view of "Threaded Multiple Path Execution" by WALLACE.

As to claims 1-6, 13, 14, and 19-25, ROTH teaches a method comprising: dynamically invoking a speculative thread (DDT thread) from a main thread (main thread) in a processor (pg. 37, "Speculative data-driven multithreading is a general purpose mechanism that expedites the execution of critical computations by allowing them to be sequenced directly while skipping over dynamically interleaved instructions from non-critical computations...When the main thread predicts an upcoming instance of a critical instruction, it forks a copy of its computation as a new kind of speculative thread."); and executing instructions comprising the speculative thread by binding a hardware context for the speculative thread (pg. 38, "The main thread forks the DDT

Art Unit: 2126

when it decodes an instance of its trigger instruction, I10 (marker 1). A new hardware context is allocated to execute the DDT and initialized with a copy of the main thread's post trigger rename map.") and transferring live-in values for pre-computation slices to hardware thread context register files (pg. 37, "However, DDMT can take advantage of a technique called register integration to allow the main thread to directly use results computed in DDTs. Integration exploits the fact that both main thread and DDT place results in a shared physical register file."). However, ROTH does not teach the system tracks for a subset of the set of loads of interest.

WALLACE teaches a thread multi-path execution system that speculatively executes threads from a main thread wherein the system tracks for a subset of the set of loads of interest the number of speculative threads that have been spawned relative to the number of instances of any load of interest that have not yet been retired by the main thread; and incrementing and decrementing the value accordingly (pg. 3, "A 2048 entry table of n-bit counters, shared among all hardware contexts, is used to keep track of the predictability of a branch..."). Therefore, it would be obvious to combine the teachings of ROTH with the teachings of WALLACE in order to determine which primary path branches to fork (pg. 3).

10. Claims 6, 7, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over TORII (U.S. Patent 6,389,446).

As to claims 6 and 7, TORII teaches transferring live-in values (thread start instruction / data) for pre-computation slices (threads) (col. 9, lines 35-55). However,

Art Unit: 2126

TORII does not teach that the transferring is through register files. Official Notice is taken in that it is well known in the art that transferring data is stored in a file or buffer and therefore would be obvious that a file or buffer of data is transferred over the bus between thread processors.

As to claim 14, refer to claim 6 for rejection.

### ***Conclusion***

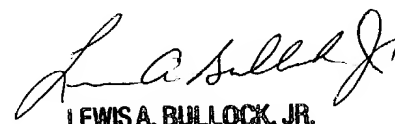
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (703) 305-0439. The examiner can normally be reached on Monday-Friday, 8:30 am - 5:00 pm. In late-October, the examiner can be reached on (571) 272-3759.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. In late-October, the examiner supervisor can be reached on (571) 272-3756.

Art Unit: 2126

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 29, 2004

  
LEWIS A. BULLOCK, JR.  
PRIMARY EXAMINER